EE / CPRE / SE 491 - sdmay20-38
iFPGA - Intermittent Intelligent FPGA Platform
Week 6 Report

10/7/19 - 10/11/19
Client: Henry Duwe
Faculty Advisor: Henry Duwe

Team Members:

Jake Tener - Team member, SW focus
Jake Meiss - Team member, HW focus
Andrew Vogler - Team member
Zixuan Guo - Team member
Justin Sung - Team member

Weekly Summary

The task this week was to continue refining the project application, and gather data on the components of the platform. These tasks were addressed by researching the SW of audio classification and performing component synthesis related to power and computational power, respectively.

Past Week Accomplishments

- FPGA HW synthesis - Justin Sung, Andrew Vogler
    - Created simple adder components to synthesize on various sizes of IGLOO nano and the IGLOO+ to determine how much computational power is utilizable on the chips.
    - Synthesis results recorded on the spreadsheet, the largest IGLOO nano is most promising so far.
- Platform/Harvester power analysis - Jake Meiss, Zixuan Guo
    - Formulated a system in order to calculate specifications such as Power consumption and output voltage, capacitance sizing, and charging/discharging times
    - Researched benefits and problems with different sizes and types of capacitors that would fulfill necessary specifications
    - Began taking measurements in the lab for RF energy harvested under different conditions
- Audio classification research - Jake Tener
    - Researched the process of audio classification and machine learning
    - Looked through past projects of audio classification to gain a better understanding of whether or not it could be replicated
    - Researched and learned Python - the language necessary for using Librosa, a very helpful sound analysis library

    - Created a program that will take a wav file in, and generate a spectrogram image of the wave file, which is a graph/picture that is frequency by time, and then the color indicates amplitude. Essentially a 3D graph.

Pending Issues

- Continue to play around with Libero SoC.

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Jake Tener	Audio classification research	8	52
Jake Meiss	Platform/Harvester power analysis	8	51
Andrew Vogler	FPGA HW synthesis	8	51
Zixuan Guo	Power requirement analysis	8	51
Justin Sung	FPGA HW synthesis	8	51

Plans for Coming Week

- Create the full audio classification SW pipeline from microphone to classification results. Once the pipeline is finished, target a specific portion of the pipeline to HW accelerate on the platform.
- Perform HW power analysis with SmartPower module of Libero SoC
- HW synthesize the IGLOO polarfire and post all FPGA comparisons to the Design Document.
- Revise the calculation process in order to take into account the minimum and maximum capacitor voltage thresholds
- Begin to research the inrush current and its possible effects on power consumption and capacitor sizing